INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

COPY OF PAPERS ORIGINALLY FILED

ATTY DOCKET NO.	SERIAL NO.
03226.102001; P[illegible]I	09/989,597
Xiao-Dong YANG, et al.	
FILING: November 20, 2001	GROUP: 2825

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

OIPE JC10 AUG 13 2002 PATENT & TRADEMARK OFFICE

RECEIVED AUG 22 2002 TECHNOLOGY CENTER 2800

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

W		A1	"A Set of Analytic Formulas for Capacitance of VLSI Interconnects of Trapezium Shape," by Ganesh Shankar Samudra and Hsio Lin Lee; IEEE Transactions on Electron Devices, Vol. 41, No. 8, August 1994; (4 pages).
W		A2	"Inductance and Capacitance Analytic Formulas for VLSI Interconnects," by N. Delorme, M. Belleville and J. Chilo; Electronics Letter, Vol. 32, No. 11, May 23, 1996; (4 pages).

EXAMINER	DATE CONSIDERED
[signature]	2-25-3

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY DOCKET NO.	SERIAL NO.
03226.102001; [illegible]91	09/989,597
Xiao-Dong YANG, et al.	
FILING: November 20, 2001	GROUP: 2825

COPY OF PAPERS ORIGINALLY FILED

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

W		B1	"Closed-Form Expressions for Interconnection Delay, Coupling and Crosstalk in VLSI's," by Takayasu Sakurai; IEEE Transactions on Electron Devices, Vol. 40., No. 1, January 1993; (8 pages).
W		B2	"Multilevel Metal Capacitance Models For CAD Design Synthesis Systems," by Jue-Hsien Chern, Jean Huang, Lawrence Arledge, Ping-Chung Li and Ping Yang; IEEE Electron Device Letters, Vol. 13, No. 1, January 1992; (4 pages).

EXAMINER	DATE CONSIDERED
[signature]	2.25.3

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.